Attorney Docket No. YO999-369

IN THE CLAIMS

Please amend the claims as follows:

Sub B1

1. (Amended) Apparatus for use in summing at least two binary values, comprising:

a binary adder circuit, responsive to a first binary value, a second binary value and a carry value, and operative to generate a binary output signal S(n) representative of a summation of the first binary value, the second binary value and the carry value, the binary adder circuit having dynamic logic, without inversion of intermediate signals prior to a final stage, for implementing an exclusive OR function that generates the binary output value without one of a positive and a negative complementary version of the carry value.

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2. (Amended) The apparatus of claim 1, wherein the binary output signal S(n) is implemented in accordance with an expression: ^(p(n) * C(n-1))*(p(n) + C(n-1)), where C(n-1) is a generate signal from a binary value n-1 associated with the carry value, p(n) is a propagate signal associated with the first binary value and the second binary value, ^ is a logical complement operator, * is an AND operator, and + is an OR operator.

Sub B1

6. (Amended) A dynamic *N*-bit parallel adder, comprising:

a first logic stage, the first logic stage configured to receive a first *N*-bit binary value and a second *N*-bit binary value and compute generate signals and propagate signals for each bit;

a second logic stage, coupled to the first logic stage, the second logic stage configured to compute block generate signals and block propagate signals for groups of one through *m* bits from the generate and propagate signals computed in the first logic stage;

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a third logic stage, coupled to the second logic stage, the third logic stage configured to combine the block generate and block propagate signals of one set of groups with the block generate and block propagate signals of another set of groups; and

a fourth logic stage, coupled to the third logic stage, the fourth logic stage configured to combine remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and to generate a summation signal wherein the summation signal

represents the logical addition of the first and second binary values and the summation signal is generated without a need for one of positive and negative complementary signal generation.

7. (Amended) The parallel adder of claim 6, wherein a generate signal and a propagate signal computed for a bit $i$ in the first logic stage represent a carry signal $c_i$, wherein $c_i$ is equivalent to $g_i + (p_i\ c_{i-1})$, where $g_i$ represents the generate signal and is equivalent to a logical multiplication operation between $a_i$ and $b_i$ where $a_i$ represents the first binary value and $b_i$ represents the second binary value, and where $p_i$ represents the propagate signal and is equivalent to a logical summation operation between $a_i$ and $b_i$.

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13. (Amended) A method of adding, in parallel, a first $N$-bit binary value and a second $N$-bit binary value, the method comprising the steps of:

computing generate signals and propagate signals for each bit;

computing block generate signals and block propagate signals for groups of one through $m$ bits from the generate and propagate signals computed in the first computing step;

combining the block generate and block propagate signals of one set of groups with the block generate and block propagate signals of another set of groups; and

combining remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and generating a summation signal wherein the summation signal represents the dynamic logical addition of the first and second binary values and the summation signal is generated without a need for one of positive and negative complementary signal generation.

14. (Amended) The method of claim 13, wherein a generate signal and a propagate signal computed for a bit $i$ in the first logic stage represent a carry signal $c_i$, wherein $c_i$ is equivalent to $g_i + (p_i\ c_{i-1})$, where $g_i$ represents the generate signal and is equivalent to a logical multiplication operation between $a_i$ and $b_i$ where $a_i$ represents the first binary value and $b_i$ represents the second binary value, and where $p_i$ represents the propagate signal and is equivalent to a logical summation operation between $a_i$ and $b_i$

operation between $a_i$ and $b_i$.

20. (Amended) A processing device having a dynamic $N$-bit parallel adder, the dynamic $N$-bit parallel adder comprising:

a first logic stage, the first logic stage configured to receive a first $N$-bit binary value and a second $N$-bit binary value and compute generate signals and propagate signals for each bit;

a second logic stage, coupled to the first logic stage, the second logic stage configured to compute block generate signals and block propagate signals for groups of one through $m$ bits from the generate and propagate signals computed in the first logic stage;

a third logic stage, coupled to the second logic stage, the third logic stage configured to combine the block generate and block propagate signals of one set of groups with the block generate and block propagate signals of another set of groups; and

a fourth logic stage, coupled to the third logic stage, the fourth logic stage configured to combine remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and to generate a summation signal wherein the summation signal represents the logical addition of the first and second binary values and the summation signal is generated without a need for one of positive and negative complementary signal generation.